miniaturization has advanced over the years are commonly expressed by their gate lengths.

The present inventors demonstrated that, when stress analysis of field-effect transistor structures is conducted and reduction of the manufacturing dimensions of the gates advances, stress generated in the interiors of the structures becomes large due to the miniaturization of the structures and the use of new materials. Particularly, in field-effect transistors which belong to the generation having a 0.1 μm gate length, stress stemming from oxidation due to STIs (Shallow Trench Isolations) becomes a source of stress.

Fig. 4 is a graph showing results in which the stress of channel portions of each generation of gate length is analyzed by the finite element method. In Fig. 4, stress generated in channel portions under the gate is low in a transistor belonging to the generation in which the gate length is a comparatively large 2 μm. However, stress becomes drastically higher in a transistor belonging to the generation in which the gate length is 0.25 μm or less, and reaches almost 3 times that of the 2 μm generation in the 0.1 μm generation. Research is being conducted in regard to the influence of stress generated in field-effect transistors on transistor characteristics. For example, research is being conducted in regard to the stress dependency of mutual conductance, which is one characteristic of field-effect transistors (Akemi Hamada, et al., IEEE Trans. Electron Devices, Vol. 38, No. 4, pp. 895-900, 1991).

However, conventionally, there was no problem of the characteristics of field-effect transistors fluctuating due to stress. This is thought to be because, as shown in Fig. 4, the stress generated in transistor structures was small in pre-0.25 μm field-effect transistors, i.e., of 0.25 μm or greater. Moreover, it is also conceivable that the sensitivity of the transistors themselves with respect to stress was also low.

Thus, when the present invention is adapted to a semiconductor device whose gate length is 0.25 μm or lower, it proves effective and is preferable.

Fig. 5 is a graph in which experimental results (gate length: 2 μm) of stress dependency of mutual conductance Gm of the aforementioned reference (Akemi Hamada, et al., IEEE Trans. Electron Devices, Vol. 38, No. 4, pp. 895-900, 1991) are compared with experimental results (gate length: 0.2 μm) of stress dependency of the mutual conductance Gm of the inventors.

The comparison in Fig. 5 was conducted by loading stress in a direction parallel to the channel with respect to n-channel field-effect transistors in which the channel was parallel to the <110> crystal axis. The dependency of Gm with respect to stress was about four times larger in the transistors of the generation in which the gate length was 0.2 μm than it was in the transistors of the generation in which the gate length was 2 μm. That is, the comparison illustrates that the sensitivity of transistor characteristics with respect to stress has become higher with the advancement of the generations of the transistors.

According to stress analysis, with respect to stress distribution in the substrate depth direction formed in the channel portion of an Si substrate of a field-effect transistor, a place at which stress concentrates is formed near the gate electrode. The diffusion zone formation region of a transistor of the generation in which the gate length is a small 0.1 μm is formed in a shallow region near the substrate surface in comparison to a conventional transistor having a large gate length. As a result, it is conceivable that, in transistors of the 0.1 μm generation, device movement regions are easily influenced by stress.

Thus, the present inventors have conducted stress analysis using the finite element method in regard to field-effect transistor structures having a gate length of 0.08 μm, and they have conducted sensitivity analysis in regard to the influence that materials configuring field-effect transistors and peripheral materials thereof exert on the stress of the channel portion in which the drain current flows. The standard dimensions (thickness) of the structures used in the sensitivity analysis were as follows. The gate length was 80 nm, the gate height was 150 nm, the film thickness

of the film enclosing the gate electrode from the upper surface thereof was 50 nm, the side wall film thickness (portions contacting the silicon substrate) was 50 nm, the silicide film thickness was 30 nm, the STI trench width was 5 μm, the STI trench depth was 350 nm, and the distance from the gate electrode to the STI was 0.62 μm. In the present specification, silicon nitride is expressed as SiN and silicon oxide is expressed as SiO_2.

As a result, the present inventors have demonstrated that the stress of the film (assuming an SiN film in the analysis) enclosing the gate electrode from the upper surface thereof and stress of the STI have a big influence on the stress of the channel portion (Fig. 6 and 7).

The present inventors have demonstrated that, in order for the stress of the channel portion to be a compression stress, the present invention could be achieved by increasing the area of the SiN, which serves as an inherent stress of compression covering the gate electrode, covering the transistor or by narrowing the STI trench width.

In light of the above-described matters, it is preferable to provide the following features.

In a semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a silicon substrate, the direction in which the drain current of the transistors mainly flows is parallel to a <100> crystal axis or to a direction equivalent to the <100> crystal axis, and the residual stress (residual strain) of the channel portion of the n-channel field-effect transistors is greater at the tensile stress side than the residual stress (residual strain) of the channel portion of the p-channel field-effect transistors.

Additionally, in a semiconductor device including n-channel field-effect transistors and p-channel field-effect transistors formed on a silicon substrate, the direction in which the drain current of the transistors mainly flows is parallel to a <100> crystal axis, or to a direction equivalent to the <100> crystal axis, the residual

stress (residual strain) of the channel portion of the n-channel field-effect transistors is tensile stress (tensile strain), and the residual stress (residual strain) of the channel portion of the p-channel field-effect transistors in a direction along the direction in which the drain current flows is compression stress (compression strain).

Thus, because the drain current characteristics of both the n-channel and the p-channel can be improved, it is possible to realize a semiconductor device that has excellent characteristics overall.

Also, the semiconductor device of the invention can realize a highly reliable semiconductor device in which defects are suppressed.

It should be noted that the axis equivalent to the <100> crystal axis is, for example, a <010> axis, a <001> axis, a <-1,0,0> axis, or a <0,-1,0> axis.

In order to achieve any of the above-described features, the following configurations are preferable.

(1) The invention is directed to a semiconductor device which includes n-channel field-effect transistors and p-channel field-effect transistors formed on a semiconductor substrate, wherein: the transistors are disposed with a gate electrode and a source and a drain corresponding thereto; the direction joining the source and the drain extends along a <100> crystal axis, or an axis equivalent to the <100> crystal axis; and compression strain is formed, in which the crystal strain of channel portions of the p-channel field-effect transistors is greater than the crystal strain of channel portions of the n-channel field-effect transistors.

Specifically, the semiconductor device is characterized in that a compression strain is formed in which the crystal strain in a direction orthogonal to the direction joining the source and the drain in a surface parallel to a gate insulating film of the channel portions of the p-channel field-effect transistors is greater than the crystal strain of channel portions of the n-channel field-effect transistors. More preferably, the semiconductor device is characterized in that, in addition to the above-described features, a compression strain in which the crystal strain in a direction orthogonal to

the direction joining the source and the drain is greater than the crystal strain of the channel portions of the n-channel field-effect transistors.

Alternatively, it can be said that the channel portions of the p-channel field-effect transistors in a direction orthogonal to the direction joining the source and the drain form a compression strain that is larger than that of the channel portions of the n-channel field-effect transistors in a direction orthogonal to the direction joining the source and the drain. More preferably, a large compression strain is also similarly formed in a direction parallel to the direction joining the source and the drain.

Thus, it is possible to improve the overall current characteristics of a semiconductor device that is disposed with n-channel field-effect transistors and p-channel field-effect transistors. Moreover, because adjustment changes of the insulating film do not influence the current characteristics, the above-described structure can effectively achieve the same effects. It should be noted that, in the semiconductor device, the insulating film may include silicon nitride as a main component.

(2) The arrangement of paragraph (1) can also be a semiconductor device characterized in that a tensile strain is formed in which the crystal strain of channel portions of the n-channel field-effect transistors is greater than the crystal strain of channel portions of the p-channel field-effect transistors.

Here, it is preferable for the direction along the axis to be parallel to the axis. However, the direction is not limited to this. It is necessary for the direction to be disposed so that the <100> axis/equivalent axis direction is closer than a direction (e.g., <110> or a direction equivalent thereto) of at least 45° to the axis. Moreover, it is even more preferable for the direction to be disposed in a range of about ±5° thereto even, if it is not strictly parallel, as described above, due to manufacturing errors and other factors.

The semiconductor device is characterized in that a tensile strain is formed in which the crystal strain in directions parallel and orthogonal to the direction joining